Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Canceled).

2. (Currently Amended) A method for creating a derivative circuit design, the method comprising:

(a) selecting an original circuit design, wherein the original circuit design comprises one or more programmable fabrics;

(b) performing front-end acceptance testing on the original circuit design, wherein front-end acceptance testing comprises

collecting data on a designer's available experiences and acceptable degree of risk,

assessing the designer's available experiences data and the designer's acceptable degree of risk data, and

accepting the original circuit design if the assessed data is within the designer's acceptable degree of risk;

(c) planning a chip layout of the accepted original circuit design;

(d) programming at least one of the one or more programmable fabrics to create a derivative circuit design; and

(e) performing verification analysis on the derivative circuit design.

3. (Previously Presented) The method of claim 2, wherein the chip layout does not exceed bounds dictated by the front-end acceptance testing.

4. (Previously Presented) The method of claim 2, further comprising

performing clocking and timing analysis prior to performing verification analysis on the derivative circuit design.

5. (Previously Presented) The method of claim 2, further comprising

performing power analysis prior to performing verification analysis on the derivative circuit design.

6. (Previously Presented) The method of claim 2, wherein only a set of new functionality added to the original circuit design and any functionality interfacing with the set of new functionality is tested or verified.

7. (Previously Presented) The method of claim 2, in which (a) through (e) are repeated to create a second derivative circuit design, wherein the derivative circuit design is used in place of the original circuit design.

8. (Previously Presented) The method of claim 2, wherein planning the chip layout comprises analyzing timing requirements to ensure the derivative circuit design meets all applicable timing requirements.

9. (Previously Presented) The method of claim 2, further comprising

assembling a chip based on the chip layout prior to performing verification analysis on the derivative circuit design.

10. (Previously Presented) The method of claim 2, wherein the original circuit design further comprises

one or more non-programmable fabrics.

11. (Previously Presented) The method of claim 2, wherein each of the one or more programmable fabrics has a port access and hierarchical routing.

12. (Previously Presented) The method of claim 10, further comprising

determining a power level for each programmable fabric and each non-programmable fabric through simulation.

13. (Currently Amended) A computer program product that includes a computer readable medium, the computer readable medium having stored thereon a sequence of instructions which, when executed by a processor, causes the processor to execute a process for creating a derivative circuit design, the process comprising:

(a) selecting an original circuit design, wherein the original circuit design comprises one or more programmable fabrics;

(b) performing front-end acceptance testing on the original circuit design, wherein front-end acceptance testing comprises

collecting data on a designer's available experiences and acceptable degree of risk,

assessing the designer's available experiences data and the designer's acceptable degree of risk data, and

accepting the original circuit design if the assessed data is within the designer's acceptable degree of risk;

(c) planning a chip layout of the accepted original circuit design;

(d) programming at least one of the one or more programmable fabrics to create a derivative circuit design; and

(e) performing verification analysis on the derivative circuit design.

14. (Previously Presented) The computer program product of claim 13, wherein the chip layout does not exceed bounds dictated by the front-end acceptance testing.

15. (Previously Presented) The computer program product of claim 13, wherein the process further comprises

performing clocking and timing analysis prior to performing verification analysis on the derivative circuit design.

16. (Previously Presented) The computer program product of claim 13, wherein the process further comprises

performing power analysis prior to performing verification analysis on the derivative circuit design.

17. (Previously Presented) The computer program product of claim 13, wherein only a set of new functionality added to the original circuit design and any functionality interfacing with the set of new functionality is tested or verified.

18. (Previously Presented) The computer program product of claim 13, in which (a) through (e) are repeated to create a second derivative circuit design, wherein the derivative circuit design is used in place of the original circuit design.

19. ((Previously Presented) The computer program product of claim 13, wherein planning the chip layout comprises

analyzing timing requirements to ensure the derivative circuit design meets all applicable timing requirements.

20. (Previously Presented) The computer program product of claim 13, wherein the process further comprises

assembling a chip based on the chip layout prior to performing verification analysis on the derivative circuit design.

21. (Previously Presented) The computer program product of claim 13, wherein the original circuit design further comprises

one or more non-programmable fabrics.

22. (Previously Presented) The computer program product of claim 13, wherein each of the one or more programmable fabrics has a port access and hierarchical routing.

23. (Previously Presented) The computer program product of claim 21, wherein the process further comprises

determining a power level for each programmable fabric and each non-programmable fabric through simulation.